Problem 1.7

For further processing an analogue signal $s(t)$ shall be digitalised to a signal $s_\mathrm{d}(k)$. The sampling frequency of the digital system is $f_\mathrm{a} = 1.024$ kHz, with a word length of 16 bit. For the quantisation a 16 bit quantiser with the maximum level of $A = \pm 1$ is implemented, which rounds the input signal-level.

1.7.1 Draw the blockdiagram of the digitalising system giving all important characteristics.

1.7.2 Give the linear model for the quantisation system.

1.7.3 Calculate the error noise power density due to the quantisation.

1.7.4 Calculate the signal-to-noise ratio for the quantisation of a sinus-shaped signal with maximal drive (i.e. $A_\mathrm{sin} = 1$).

At the input of the system a very weak sine shall be measured. The amplitude of the signal is $A = 2^{-15}$ whereby its frequency is $f_0 = 64$ Hz.

1.7.5 Sketch the power density spectrum of the input signal.

1.7.6 Sketch the output signal of the quantiser.

1.7.7 Calculate and sketch the power density spectrum of the output signal.

1.7.8 Describe a possible method to reduce the distortions of the output signal due to the low signal level at the input.

Problem 1.8

For further processing an analogue signal $s(t)$ shall be digitalised to a signal $s_\mathrm{d}(k)$. The digitalisation shall be done with a one-bit delta-sigma modulator. The sampling frequency of the digital system is f_a. For the quantisation the maximum level of $A = \pm 1$ shall be assumed.

1.8.1 Describe the delta modulator.

1.8.2 Develop from the delta modulator a sigma-delta modulator.

1.8.3 Calculate the difference equation of the sigma-delta modulator.

1.8.4 Calculate and sketch the power density spectrum the quantisation error.