**Closed-Loop Real-Time MIMO-OFDM System for Adaptive Transmissions**

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**Introduction**

- High spectral efficiency communications set stringent requirements on the signal quality, specially in the AFE. Rapid-prototyping of new MIMO processing algorithms requires a good hardware and software partition. Adaptive MIMO-OFDM algorithms with transmit CSI require real-time processing and feedback signalization.

- The present system implements an explicit feedback link in the form of a logical channel (over TCP/IP). No physical connection between the transmitter and receiver is required.

- The design targets a signal quality of KVM = -35, using the transmission parameters of IEEE 802.11a.

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**Adaptive MIMO with bit-loading**

MIMO OFDM permits reliable communications in poor propagation conditions by space-frequency diversity, and higher data rate transmissions in good propagation conditions by spatial multiplexing. Implementing adaptive techniques (e.g. bit-loading, adaptive modulation and coding, and adapting the MIMO technique) results in significant gains in throughput and reliability over non-adaptive systems.

**Transmitter Features**

- Fixed-point DSP for fast and flexible programming of transmit signal adaption and frequency-domain MIMO transmit processing.
- FPGA for OFDM modulation (64-point pipelined FFT and cyclic prefix addition), preamble addition and digital up-conversion to 30MHz.
- Analog front-end characteristics:
  - 16-bit D/A converters operating at 60MHz.
  - Sampling and carrier oscillators common in all antenna branches, derived from a very precise reference with very small phase noise.
  - Working point of the power amplifier is set such that non-linearities can be neglected.
- The signal is transmitted with 6dBm in power over 4 antennas separated by a distance of 15 cm.

**FPGA Utilization**

<table>
<thead>
<tr>
<th>Target device</th>
<th>xc2v4000-5ff1152</th>
</tr>
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<tbody>
<tr>
<td>Internal word length</td>
<td>12 bits</td>
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<tr>
<td>External word length</td>
<td>12 bits</td>
</tr>
<tr>
<td>Slice flip-flops</td>
<td>14169 (30%)</td>
</tr>
<tr>
<td>Block RAMs (18Kbit)</td>
<td>26 (23%)</td>
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<tr>
<td>Embedded multipliers</td>
<td>16 (13%)</td>
</tr>
<tr>
<td>Clock frequency constraint</td>
<td>60 MHz</td>
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<tr>
<td>Optimization goal</td>
<td>Minimum area</td>
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</table>

**Description**

- Detection order based on $|b_1|^2$ and $|b_2|^2$.
- First detection: matrix inversion.
- Second detection: Micro-Parsec matrix pseudo-inversion reduces MRC.

**Features**

- Processing delay (48 used subcarriers per OFDM symbol):
  - MIMO channel estimation: 12µs.
  - Detection of two streams using 64QAM (worst-case): 49µs.
- Signal quality (measured by the error vector magnitude):
  - Single antenna transmissions: EVM = 23dB.
- Multiple antenna transmissions: EVM = 25dB.
- Raw data rate is 144Mbps, for a spectral efficiency of 12 uncoded bits / subcarrier.

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**Adaptive Transmitter Architecture**

**Adaptive Receiver Architecture**

**Real-Time Signal Adaptation by Bit-Loading**

**Rapid-Prototyping of the VBLAST Algorithm**

Computational-efficient implementation of subcarrier-based VBLAST detection for 2 × 2 MIMO systems.

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**Resource**

- Target device: xc2v4000-5ff1152
- Internal word length: 12 bits
- External word length: 12 bits
- Slice flip-flops: 14169 (30%)
- Block RAMs (18Kbit): 26 (23%)
- Embedded multipliers: 16 (13%)
- Clock frequency constraint: 60 MHz
- Optimization goal: Minimum area

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**Receiver Features**

- Analog front-end characteristics:
  - Signal received by 4 antennas is transmitted over 15cm.
  - 16-bit D/A converters operating at 60MHz.
  - Sampling and carrier oscillators common in all antenna branches are derived from a very accurate reference that is independent from the one used at the transmitter.
- FPGA for digital-downconversion to baseband, frame synchronization and OFDM demodulation (cyclic prefix suppression and FFT).
- Fixed-point DSP for fast and flexible programming of frequency-domain MIMO receiver processing, extraction of adaptive parameters and communication detection.
- In closed-loop mode, communication parameters are extracted and fed back to the transmitter for link adaptation.

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**Resource**

- Target device: xc2v4000-5ff1152
- Internal word length: 14 bits
- External word length: 12/10 bits
- Slice flip-flops: 11218 (24%)
- Block RAMs (18Kbit): 38 (26%)
- Embedded multipliers: 31 (25%)
- Clock frequency constraint: 60 MHz
- Optimization goal: Minimum area

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**Description**

- Indoor transmissions with rich scattering (walls, furniture, people) are frequency-selective.
- The power of the transfer factors shows large variations in different sub-carriers and antenna paths.
- The signal quality can be largely improved by adaptive techniques (such as bit-loading) requiring feedback information in real time.

**Comparison**

- First transmit antenna: uniform modulation (BPSK). EVM = 23dB.
- Second transmit antenna: information is bit-loaded over subcarriers at the same data rate. EVM = 26dB.
- Gain in signal quality: 5dB.
- Processing delay of the bit-loading algorithm: 34µs / data stream.