Closed-Loop Real-Time MIMO-OFDM System for Adaptive Transmissions

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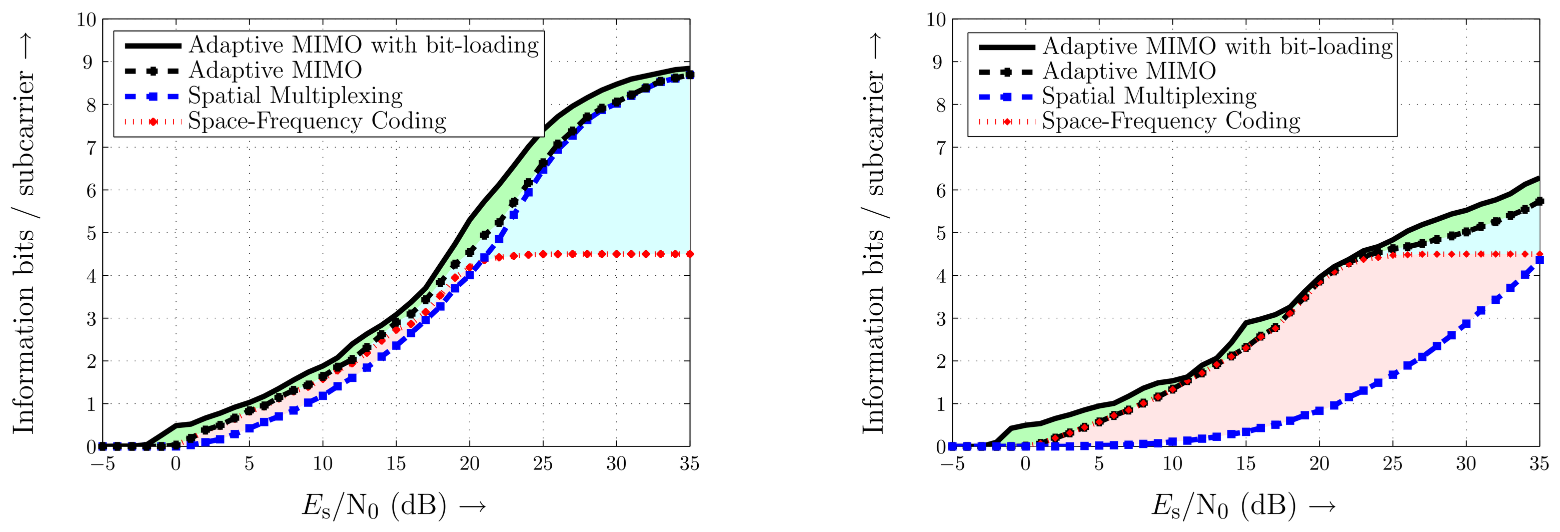
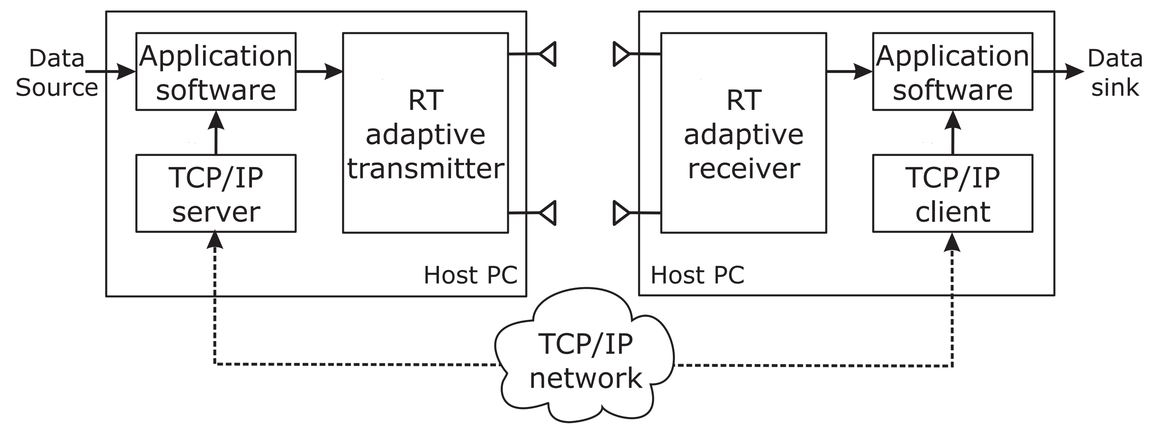
Introduction

- MIMO-OFDM permits reliable communications in poor propagation conditions by space-frequency diversity, and higher data rate transmissions in good propagation conditions by spatial multiplexing.
- Implementing adaptive techniques (*e.g.* bit-loading, adaptive modulation and coding, and adapting the MIMO technique) results in significant gains in throughput and reliability over non-adaptive systems.



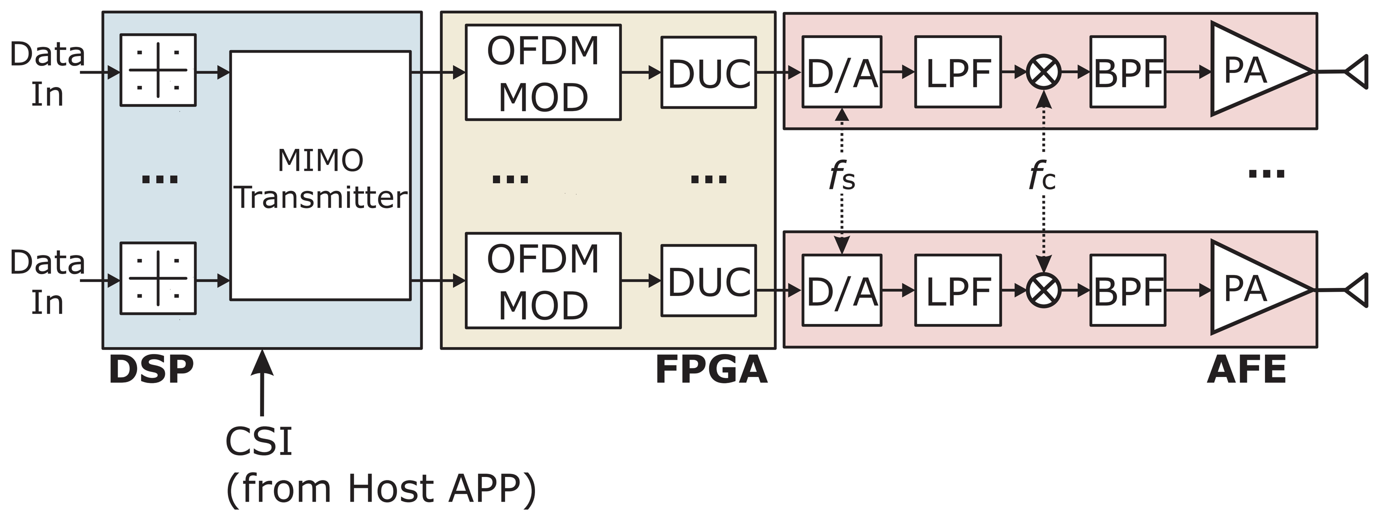
Throughput of adaptive 2 × 2 MIMO BICM OFDM systems in indoor and outdoor transmissions.

- High spectral efficiency communications set stringent requirements on the signal quality, specially in the AFE.
- Rapid-prototyping of new MIMO processing algorithms requires a good hardware and software partition.
- Adaptive MIMO-OFDM algorithms with transmit CSI require real-time processing and feedback signalization.

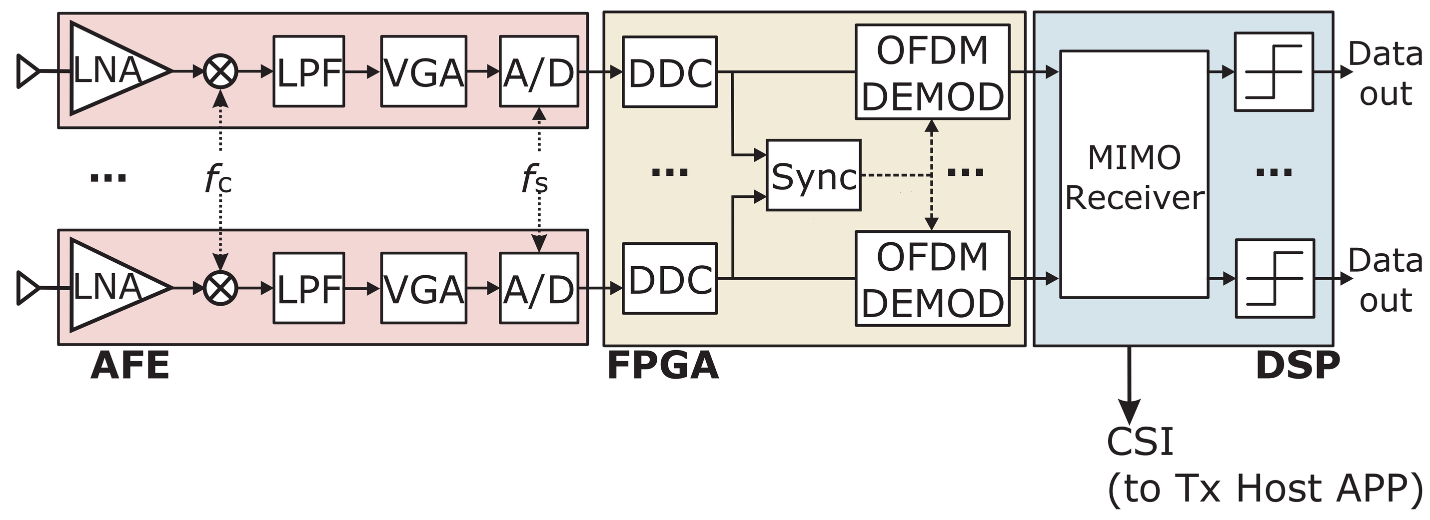


- The present system implements an *explicit* feedback link in the form of a logical channel (over TCP/IP). No physical connection between the transmitter and receiver is required, therefore their location is of no concern.
- The design targets a signal quality of EVM = -35, using the transmission parameters of IEEE 802.11a

Adaptive Transmitter Architecture



Adaptive Receiver Architecture



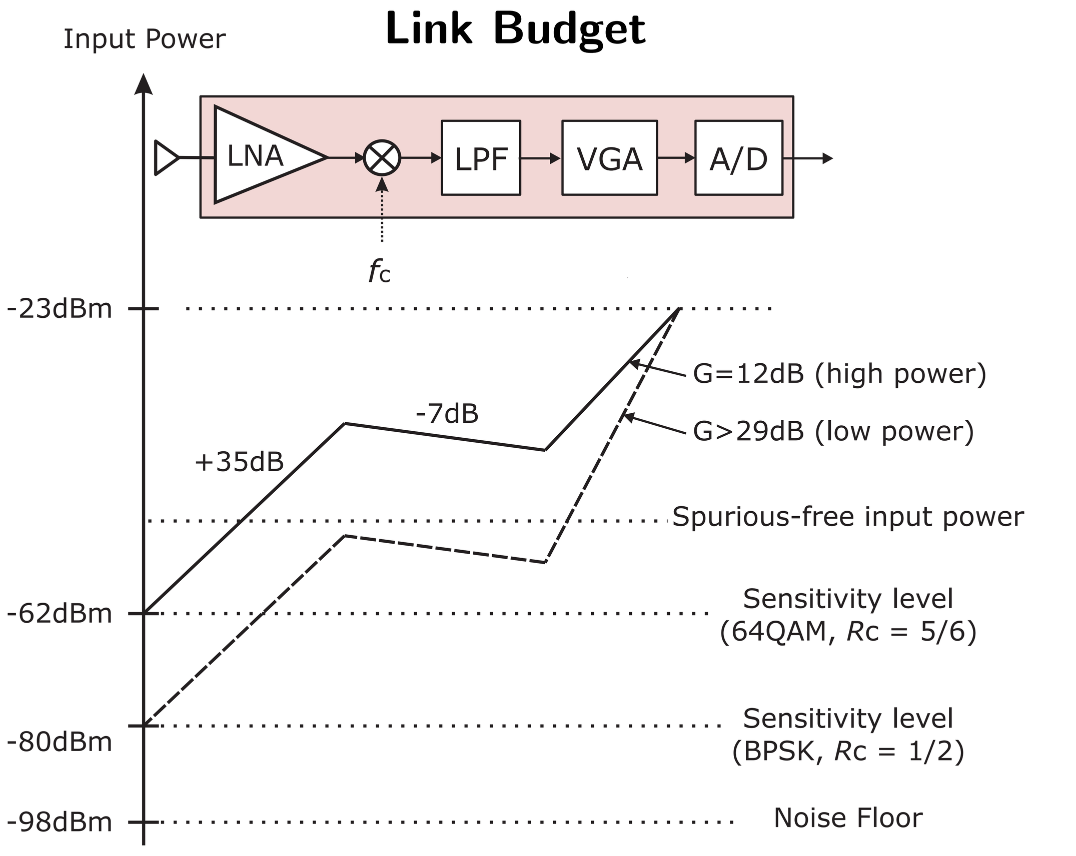
Transmitter Features

- Fixed-point DSP for fast and flexible programming of transmit signal adaption and frequency-domain MIMO transmit processing.
- FPGA for OFDM modulation (64-point pipelined IFFT and cyclic prefix addition), preamble addition and digital up-conversion to 16MHz.
- Analog front-end characteristics:
  - 16-bit D/A converters operating at 60MHz.
  - Sampling and carrier oscillators common in all antenna branches, derived from a very precise reference with very small phase noise.
  - Working point of the power amplifier is set such that non-linearities can be neglected.
  - The signal is transmitted with 0dBm in power over $\lambda/4$ monopole antennas separated by a distance of 15 cm.

FPGA Utilization

Resource	
Target device	xc2v4000-5ff1152
Input word length	8 bits
Internal word length	12 bits
Slice flip-flops	14196 (30%)
Block RAMs (18Kbit)	26 (21%)
Embedded multipliers	16 (13%)
Clock frequency constrain	60 MHz
Optimization goal	Minimize area

Link Budget



- Average input power to the A/D converter:

$$P_{\mathrm{A/D}} = \frac{V_{\mathrm{clip}}^2}{(\sqrt{2}B_o)^2 R_{\mathrm{in}}} = -23\mathrm{dBm}.$$

- Sensitivity for BPSK with $R_c = 1/2$ defines the largest VGA gain.
- Sensitivity for 64QAM with $R_c = 5/6$ determines the VGA's IIP3.
- Analog components selected such that non-linearities do not affect the signal quality. The maximum spurious-free input power is:

$$P_{\mathrm{in}} = \frac{2IIP3 - 174 + 10\mathrm{Log}(B) + NF - 10\mathrm{Log}(N/2)}{3} = -54\mathrm{dBm}$$

Receiver Features

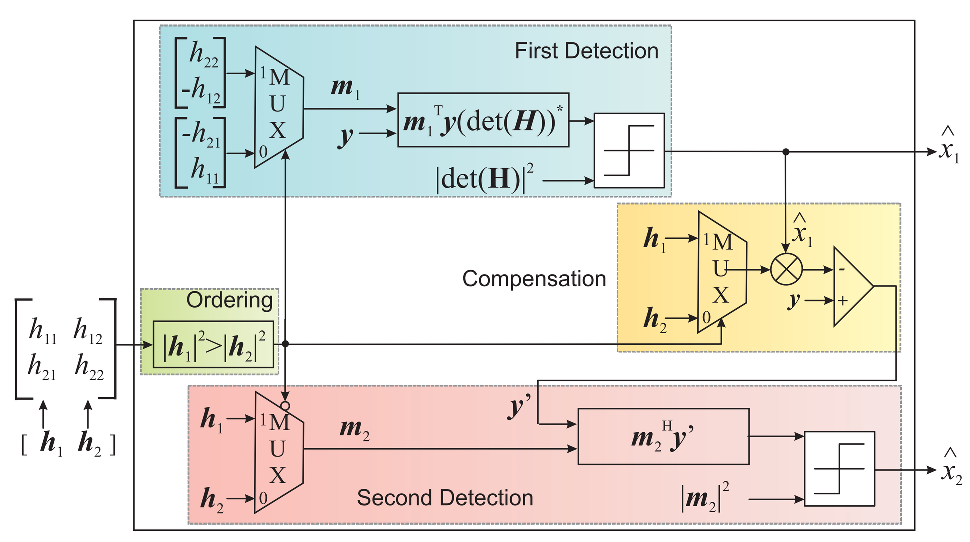
- Analog front-end characteristics:
  - Signal received by $\lambda/4$ monopole antennas separated by 15cm.
  - 14-bit A/D converters operating at 60MHz.
  - Sampling and carrier oscillators in all antenna branches are commonly derived from a very accurate reference that is independent from the one used at the transmitter.
- FPGA for digital down-conversion to baseband, frame synchronization and OFDM demodulation (cyclic prefix supression and FFT).
- Fixed-point DSP for fast and flexible programming of frequency-domain MIMO receive processing, extraction of adaptive parameters and constellation detection.
- In closed-loop mode, communication parameters are extracted and fedback to the transmitter for link adaption.

FPGA Utilization

Resource	
Target device	xc2v4000-5ff1152
Input word length	14 bits
Internal word length	12/10 bits
Slice flip-flops	11218 (24%)
Block RAMs (18Kbit)	30 (25%)
Embedded multipliers	31 (25%)
Clock frequency constrain	60 MHz
Optimization goal	Minimize area

Rapid-Prototyping of the VBLAST Algorithm

Computational-efficient implementation of subcarrier-based VBLAST detection for 2 × 2 MIMO systems.

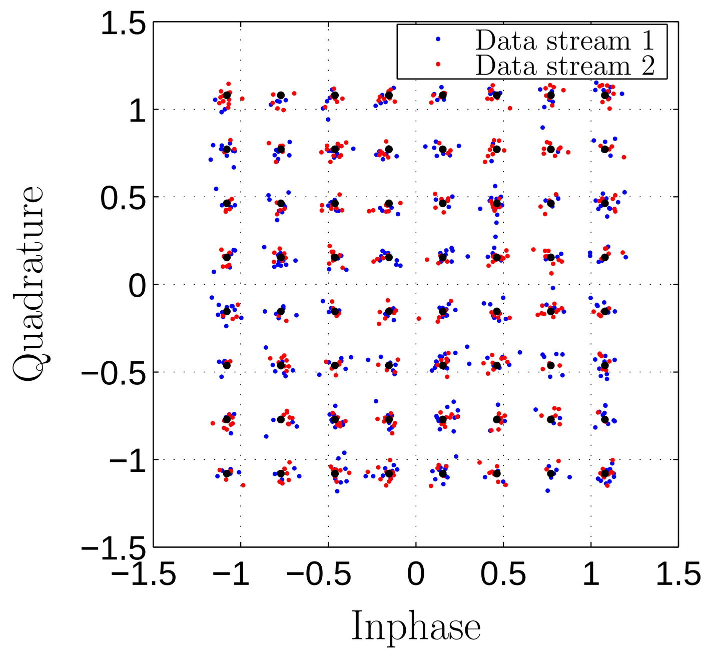


Description

- Detection order based on $|\mathbf{h}_1|^2$ and $|\mathbf{h}_2|^2$.
- First detection: matrix inversion.
- The interference caused by the first data stream is compensated before the second detection.
- Second detection: Moore-Penrose matrix pseudo-inversion reduces to MRC.

Features

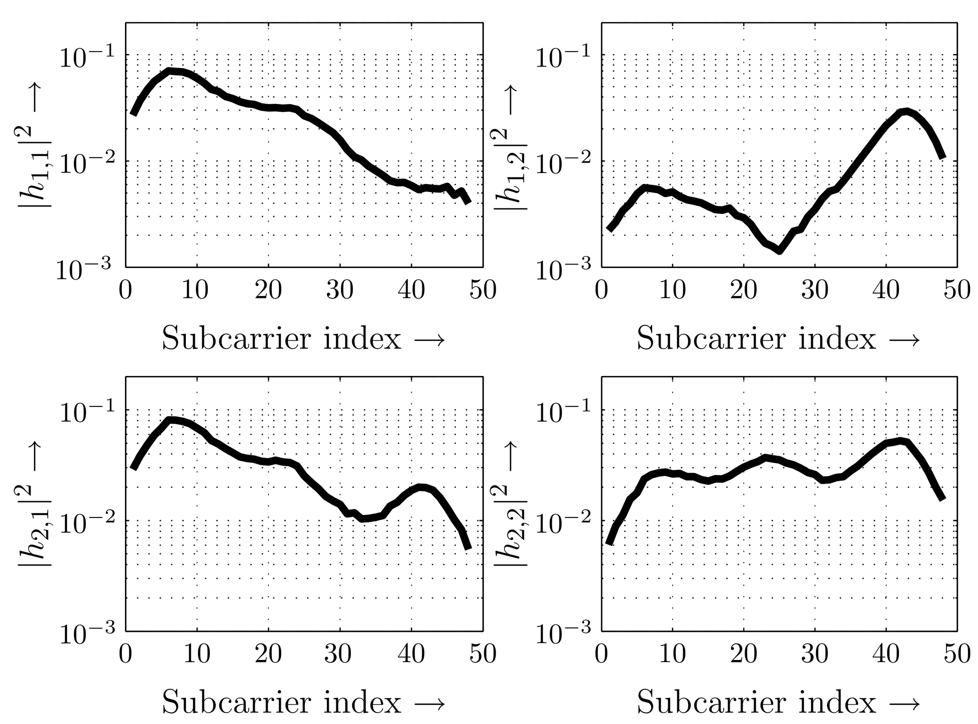
- Processing delay (48 used subcarriers per OFDM symbol):
  - MIMO channel estimation: 110μs.
  - Detection of two streams using 64QAM (worst-case): 400μs.
- Signal quality (measured by the error vector magnitude):
  - Single antenna transmissions: EVM = -32dB.
  - Multiple antenna transmissions: EVM = -25dB.
- Raw data rate is 144Mbps, for a spectral efficiency of 12 uncoded bits / subcarrier.



Real-Time Signal Adaptation by Bit-Loading

Description

- Indoor transmissions with rich scattering (walls, furniture, people) are frequency-selective.
- The power of the transfer factors shows large variations in different subcarriers and antenna paths.
- The signal quality can be largely improved by adaptive techniques (such as bit-loading), requiring feedback information in real time.



Comparison

- First transmit antenna: uniform modulation (BPSK); EVM = -21dB.
- Second transmit antenna: information is bit-loaded over subcarriers at the same data rate; EVM = -26dB.
- Gains in signal quality: 5dB.
- Processing delay of the bit-loading algorithm: 34μs / data stream.